What is claimed is:

1. An interconnect structure, comprising:

a substrate;

a first metal line disposed on the substrate;

a first insulating layer disposed on the substrate, covering the first metal line;

a second metal line disposed on the first insulating layer;

a second insulating layer covering the second metal line;

ITO (indium tin oxide) wiring electrically connecting the first and second metal lines; and

a passivation structure disposed on the second insulating layer with an opening therein to expose and enclose the ITO wiring.

2. The interconnect structure as claimed in claim 1, wherein the substrate is a TFT-array substrate for a flat display panel.

3. The interconnect structure as claimed in claim 1, wherein the first and second metal lines, the ITO wiring and the passivation structure are disposed in a non-display area of the TFT-array substrate.

4. The interconnect structure as claimed in claim 3, wherein the first metal line is a gate metal line formed simultaneously with gate metal lines in a display area of the TFT-array substrate.

5. The interconnect structure as claimed in claim 3, wherein the second metal line is a source/drain metal line that is formed simultaneously with source/drain metal lines on a display area of the TFT-array substrate.

6. The interconnect structure as claimed in claim 1, wherein the ITO wiring comprises a first ITO electrode disposed in the first and second insulating layers in contact with the first metal line, a second ITO electrode disposed in the second insulating layer in contact with the second metal line, and an ITO layer connecting the first and second ITO electrodes.

7. The interconnect structure as claimed in claim 1, wherein the thickness of the passivation structure is between 3 and 4μm.

8. The interconnect structure as claimed in claim 1, wherein the opening in the passivation structure is rectangular.

9. A method for fabricating an interconnect structure on a TFT-array substrate of a flat panel display, comprising:

forming a plurality of first metal lines in a non-display area of the TFT-array substrate;

forming a first insulating layer on the TFT-array substrate to cover the first metal lines;

forming a plurality of second metal lines on the first insulating layer, wherein each second

metal line corresponds with one first metal line;

forming a second insulating layer covering the second metal lines and the first insulating layer;

forming a passivation structure on the second insulating layer with openings therein to expose one end of every first and its corresponding second metal lines;

forming a plurality of first and second via holes in the first and second insulating layers inside the opening of the passivation structure to expose the first and second metal lines respectively;

forming an ITO (indium tin oxide) layer on the second insulating layer, filling the first and second via holes to connect the first and second metal lines;

forming a patterned photoresist layer on the ITO layer, masking the ITO layer inside the opening of the passivation structure;

etching the ITO layer with the patterned photoresist layer as a mask to form ITO wiring to connect the first metal line with the second metal line; and

removal of the remaining photoresist layer.

10. The method as claimed in claim 9, wherein the first metal line is formed simultaneously with gate metal

lines formed in a display area of the TFT-array substrate.

11. The method as claimed in claim 9, wherein the second metal line is formed simultaneously with source/drain metal lines formed in a display area of the TFT-array substrate.

12. The method as claimed in claim 9, wherein the thickness of the passivation structures is between 3 and 4μm.

13. The method as claimed in claim 9, wherein the opening of the passivation structure is rectangular.